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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,531	02/13/2002	David Nguyen	1726.7221200	8963

7590 06/02/2005

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EXAMINER	
NGUYEN, MINH T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,531	NGUYEN ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,8-11 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,8-11 and 16-20* is/are rejected.

7)☒ Claim(s) *21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 3/15/05 has been received and entered in the case. Claims 1-4, 8-11 and 16-22 are pending. The amendment and argument presented therein overcome the prior art rejections noted in the previous Office action, and therefore, these are withdrawn. New grounds of rejections necessitated by the amendment are needed as set forth below. This action is FINAL.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 8-11, 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,742,798, issued to Goldrian.

As per claim 1, Goldrian discloses a method for accommodating transition-induced delay (Figs. 5A and 5B) comprising the steps of:

determining a first relationship between a current logic state and a next logic state (column 4, lines 46-48 and column 4, lines 66-67, i.e., the state of the delayed clock signal (511) is detected at every positive transition of the reference clock signal (520), the change regarding the previous state is output at the output (516) of flip-flop 512, column 5, lines 1-7. In other

words, the relationship of the delay clock 511 before the positive transition of the reference clock signal and after the positive transition of the reference clock signal are determined, the result is output on line 516 of flip-flop 512) of a first clock signal CLOCK; and

adjusting a first delay of a first clock signal based on at least in part upon the first relationship by controlling at least one delay element (column 5, lines 11-12, i.e., the information on the output of the flip-flop 512 is used to quantify delay information, the recited at least one delay element reads on the combination of elementary delays 502, the selector 508 controls the taps of the at least one delay element).

Goldrian does not disclose the signal to be adjusted is a data signal as called for in the claim. However, as known by a person skilled in the art, clock signal is merely a special kind of data signal when these signals are digital. Further evidence can be found in figure 1 of the applicant's admitted prior art.

It would have been obvious to one skilled in the art at the time of the invention was made to use the apparatus shown in figure 5 of Goldrian for accommodating transition induced delay of data signal instead of clock signal. The motivation and/ or suggestion would be to take advantage of the known structure for use in applications which call for quantifying the delay information of data signal instead of a clock signal since it is clear that there is no distinguish whether the data signal or clock signal is used in the Goldrian's apparatus shown in figure 5A.

As per claim 2, Goldrian further discloses determining a second relationship between current logic state and a next logic state of a second line (Fig. 2, the first relationship is on chip A 204 and the second relationship is on chip B 205) wherein the step of adjusting the first delay of the first data signal based at least in part upon the first relationship further comprises the step of:

adjusting the first delay of the first data signal based at least in part upon the first and second relationships (shown as the loop, i.e., arrow from chip A to chip B and from chip B to chip A, Fig. 3, the delay information from chip B is transfer backed to chip A).

As per claim 3, the recited limitation is shown in Fig. 6 and described in column 5, lines 13-45. Further, as shown in Fig. 2, the first delay is adjusted by varying the delay of the variable clock delay A 206 and the second delay is adjusted by varying the delay of the variable clock delay B 207.

As per claim 4, the recited limitation is described in column 5, lines 4-12, i.e., when the current logic state is similar to the next logic state, phase reversal happens. In other words, more delay should be provided.

As per claim 8, Goldrian discloses an apparatus (Fig. 10) for accommodating transition-induced delay comprising:

a transition detection block (the combination of each of the transition detection circuits in each of the chips M1, ..., N3, the details of two are shown in Fig. 2 and discussed in claim 1 herein above) having a plurality of inputs (as shown in Fig. 5, each has an input delay clock 511), for receiving a corresponding a plurality of clock signals (also as shown in Fig. 5, each line in each chip carries an input delay clock 511), the transition detection block detecting transitions of the plurality of clock signals (discussed in claim 1); and

a delay adjustment block (the combination of each of the delay adjustment circuits in each of the chips M1, ..., N3, the details of two, variable clock delay A and variable clock delay B, are shown in Fig. 2) coupled to the transition detection block, the delay adjustment block

adjusting a delay in at least one of the plurality of data signals by controlling at least one delay element (discussed in claim 1).

Goldrian does not explicitly disclose signals to be adjusted are data signals as called for in the claim. However, using data signals instead of clock signals are seen as obvious for the reasons and motivation discussed in claim 1.

As per claim 9, shown in Fig. 5, the transitions from first to second levels or second to first levels are detected at every positive transition of the reference clock (column 4, lines 66-67).

As per claim 10, this claim is rejected for the same reason noted in claim 3.

As per claim 11, the recited limitation is merely a defined relationship based on the results displayed at each of the outputs of the transition detection circuits. Because such a defined relationship resulted in no structural difference between the claimed apparatus and the reference apparatus, the recited limitation is met. See MPEP 2114.

As per claim 16, this claim is merely a method to operate the apparatus having the structure noted in claim 8, since Goldrian teaches the circuit, he inherently teaches the method.

As per claims 17-19, these claims are rejected for the same reasons noted in claims 9-11, respectively.

As per claim 20, the recited limitation is met because when the number of same level transitions are different, the clocks are skewed different, therefore, the adjustment for each must be different.

Response to Arguments

3. Applicant's arguments filed on 3/15/05 have been fully considered but they are not persuasive.

Regarding the argument that Goldrian is directed to clock signals whereas the claim call for data signals.

This argument is moot in view of new ground of rejection.

Regarding the argument that Goldrian only discloses the determination of the number of elementary delays whereas the claim calls for adjusting a first delay based at least in part upon the first relationship by controlling at least one delay element.

As discussed in the preceding rejection, the determination of the first relationship is disclosed in column 4, lines 46-48 and column 4, lines 66-67, i.e., the state of the delayed clock signal (511) is detected at every positive transition of the reference clock signal (520), and the change regarding the previous state is output at the output (516) of flip-flop 512 (column 5, lines 1-7). In other words, the relationship of the delay clock 511 before the positive transition of the reference clock signal and after the positive transition of the reference clock signal are determined, the result is output on line 516 of flip-flop 512.

The recited controlling is performed by the selector 508 shown in figure 5A. The recited controlling at least one delay element is met when considering the combination of elementary delays 502 is the recited "at least one delay element", i.e., the selector 508 controls the taps of the "at least one delay element".

Allowable Subject Matter

4. Claims 21-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 21-22 are allowable because the prior art of record fails to disclose or suggest the step of adjusting the delay based on the comparisons of the difference in numbers of each level transitions to a threshold as recited in claim 21.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/27/05

Minh Nguyen
Primary Examiner
Art Unit 2816